Output-Determinacy and Asynchronous Circuit Synthesis

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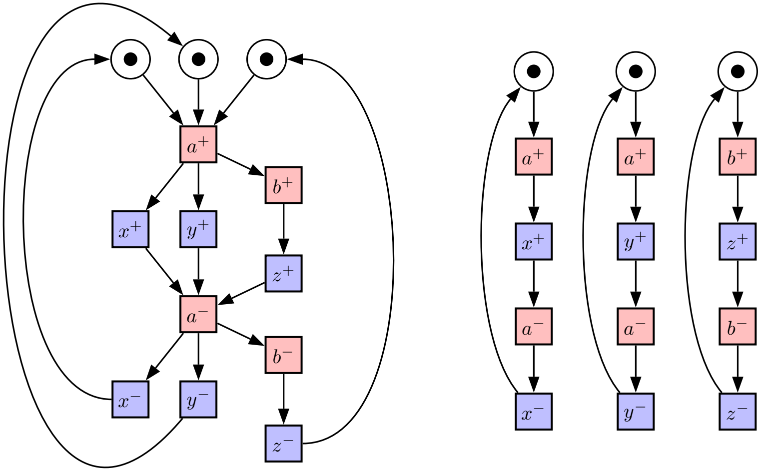
ACSD 2007

Decomposition and Correctness



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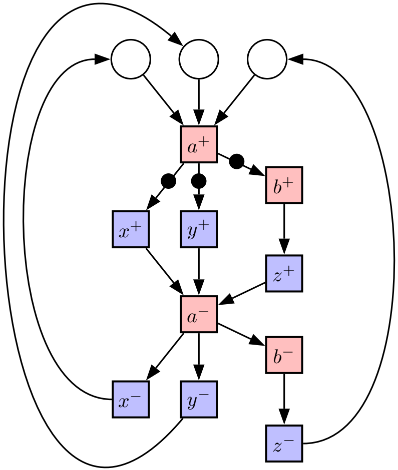

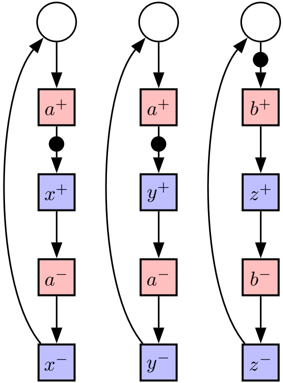

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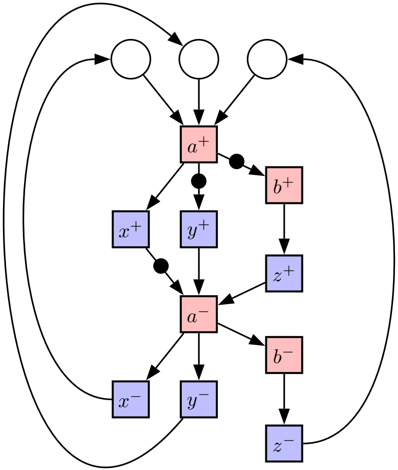

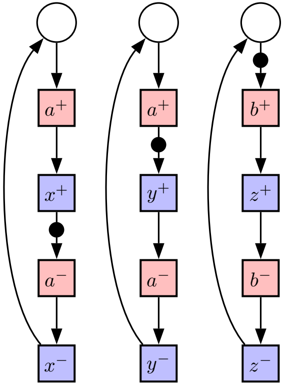

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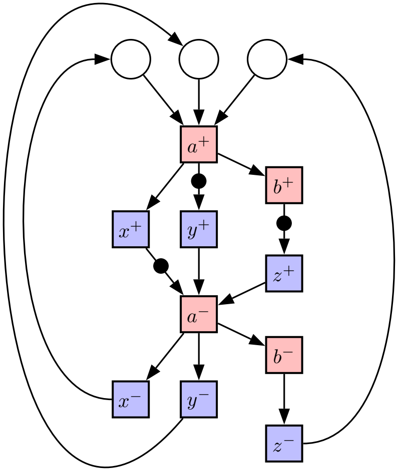

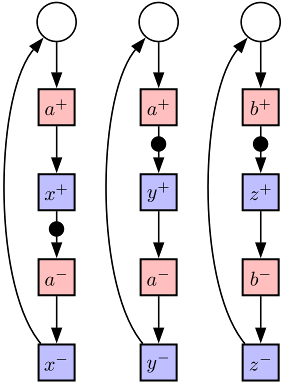

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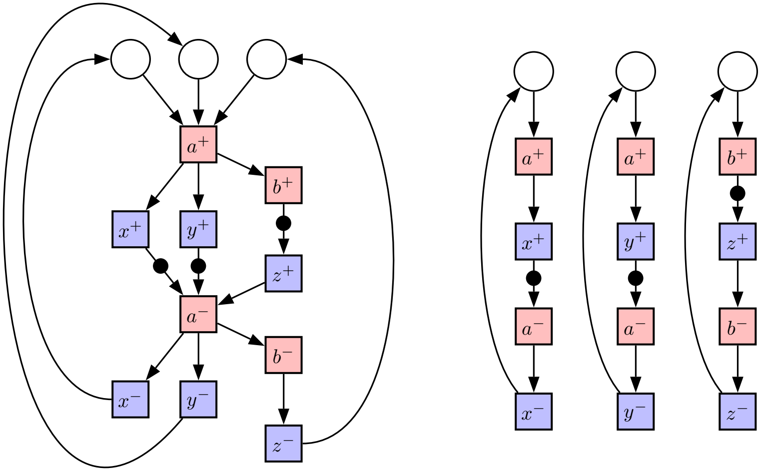

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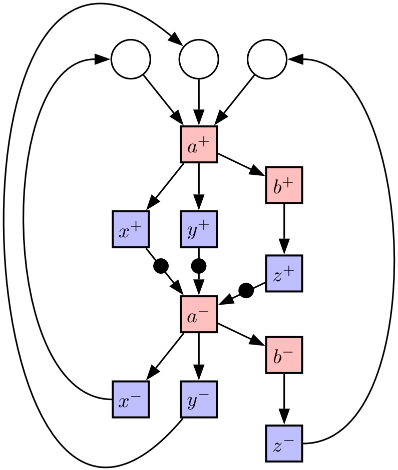

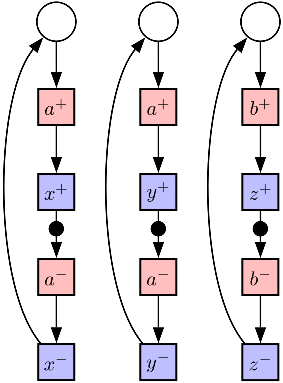

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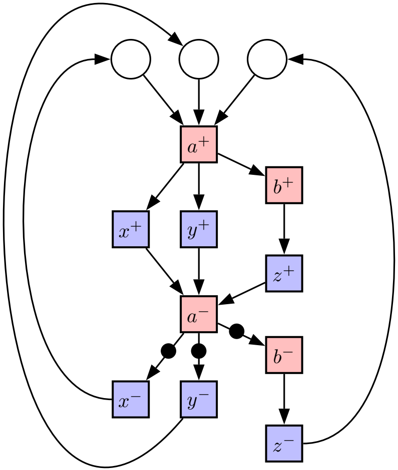

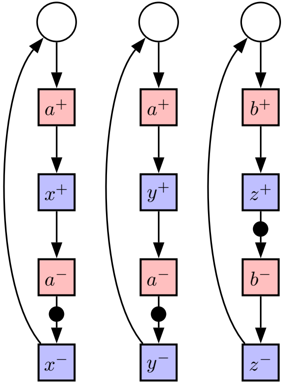

Advantage of Decomposition

- Concurrency is typical for asynchronous circuits, but leads to state explosion
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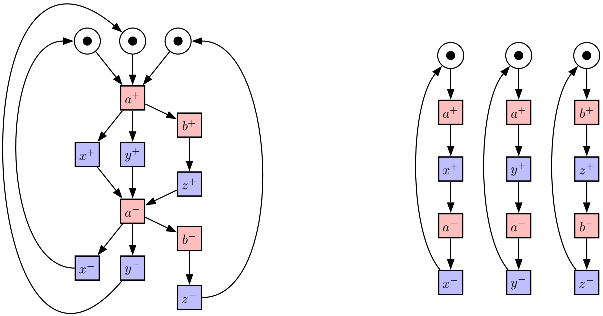

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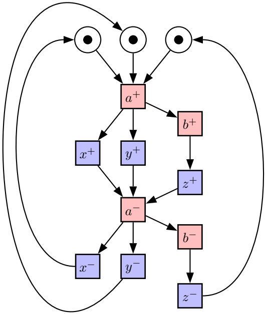
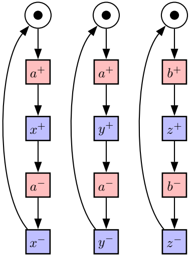
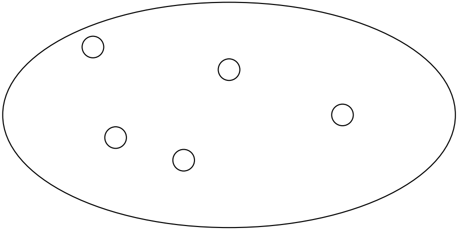


24 states



4 states each

Determinism



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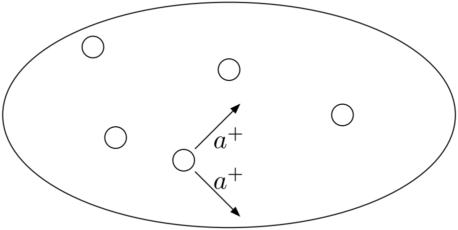

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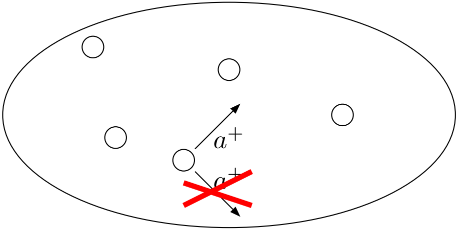

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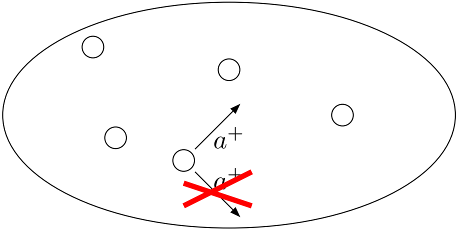

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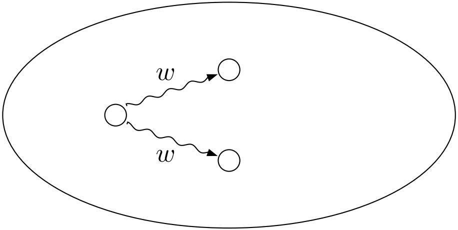

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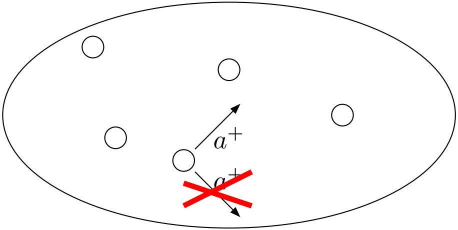

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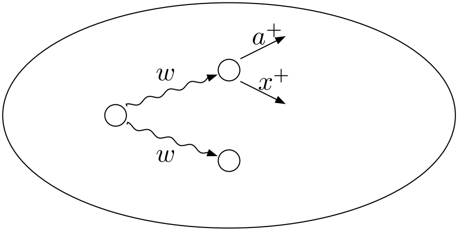

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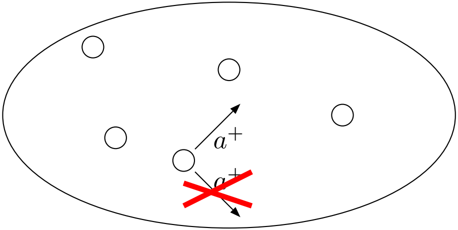

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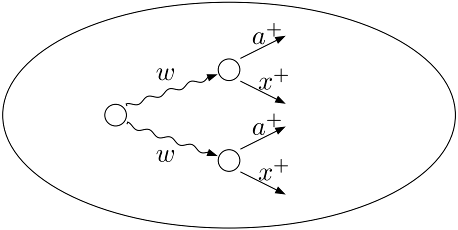

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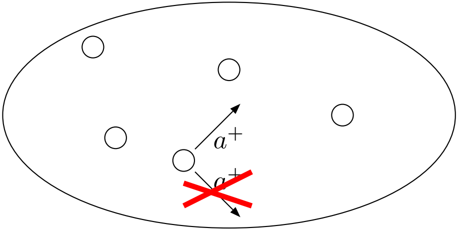

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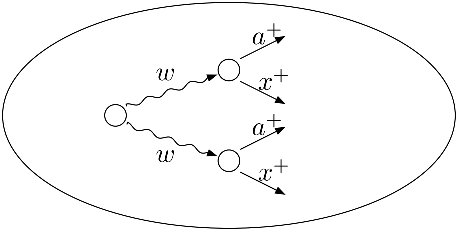
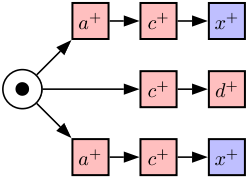
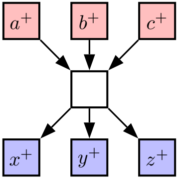
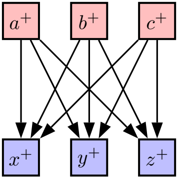




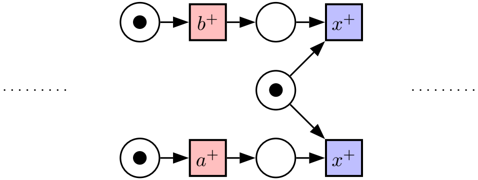
Dummy transitions are like λ/ϵ edges in an automaton.
Inserted for convenience.



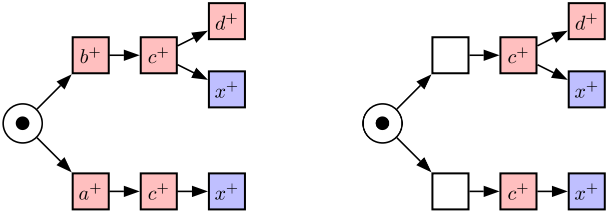


3 outputs are triggered by three inputs
left: 6 places and 1 transitions – right: 9 places

If an action x^+ should occur after the action a^+ **or** b^+ occurs, one has to use either unsafe or non-deterministic STGs. However, unsafe STGs are not preferable in praxis.

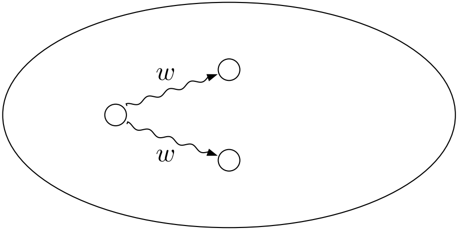


Hiding of signals, i.e. labelling them with λ. Essential operation of our STG decomposition algorithm.



Hiding of *a* and *b*

Output-Determinacy – Definition



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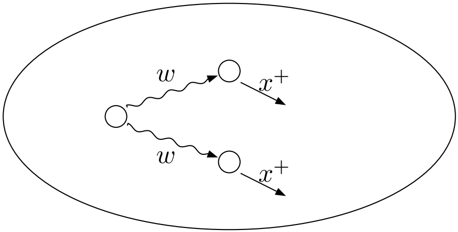

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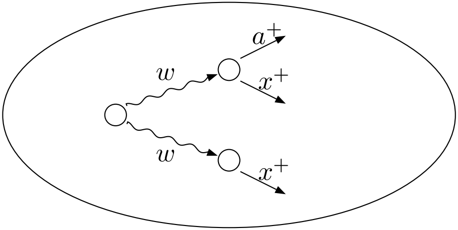

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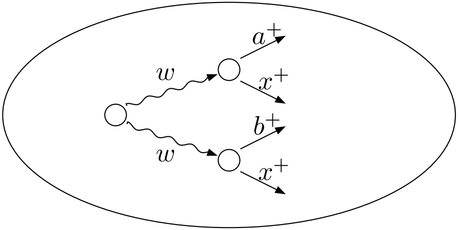

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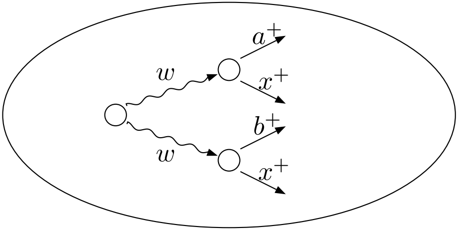

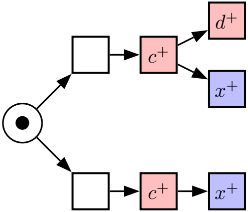

Output-Determinacy – Why not Determinise?

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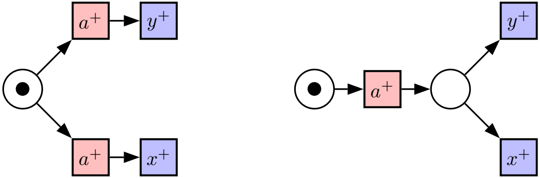
  - Violation of semi-modularity
  - Violation of correctness

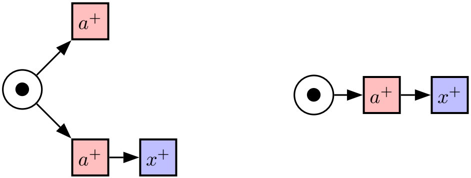
Violation of Semi-Modularity



left: non-output-determinate: STG
right: determinised version, x^+ is in conflict with y^+

Output-Determinacy – Why not Determinise?

Violation of Correctness



left: non-output-determinate: STG
right: determinised version, can be synthesised but is not correct

Output-Determinacy – CSC Conflicts

- Non-output-determinacy is also a CSC conflict
- CSC conflicts can be resolved by insertion of internal signals in a behaviour-preserving way
- Does not work for violation of output-determinacy

Output-Determinacy – Justification

A non-output-determinate specification is ill-formed and cannot be implemented speed-independently.

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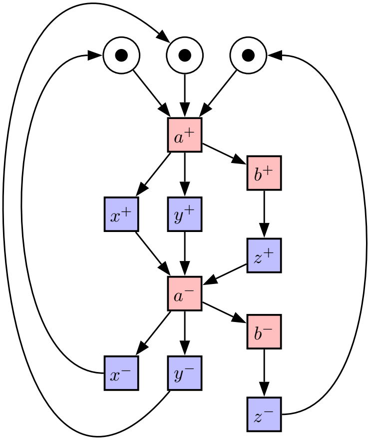
These give a semantics for non-deterministic specifications.

Decomposition – Example



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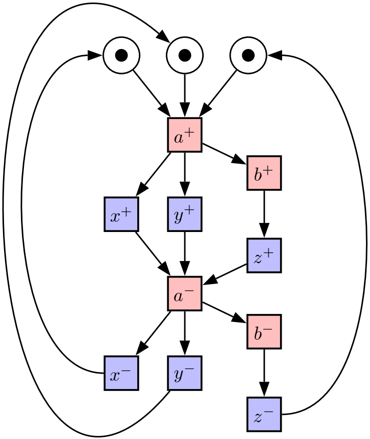

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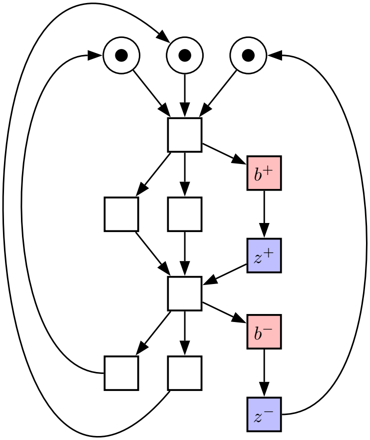

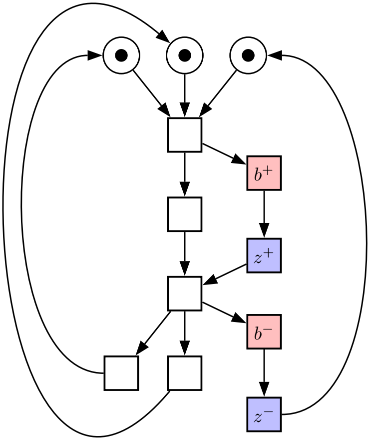

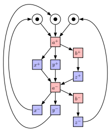

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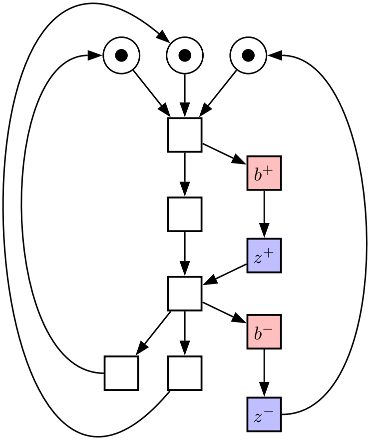

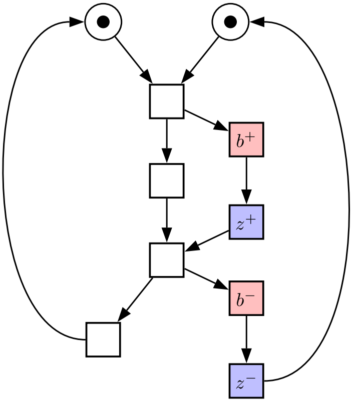

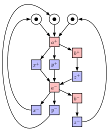

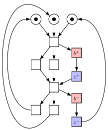

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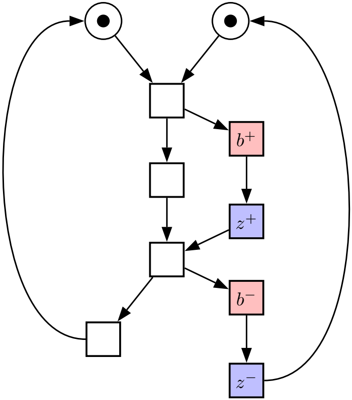

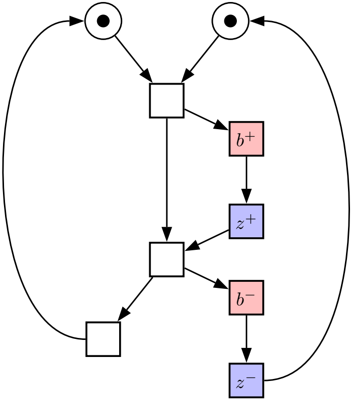

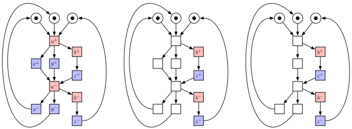

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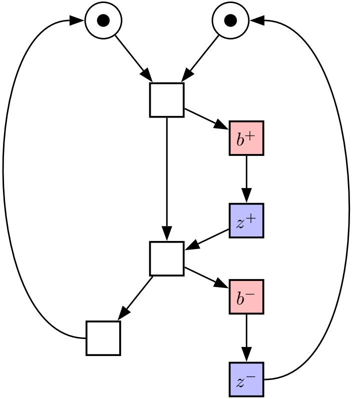

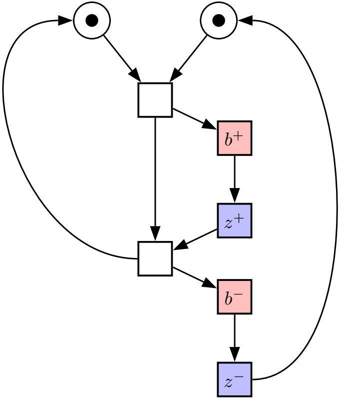

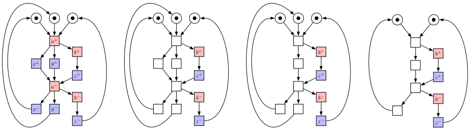

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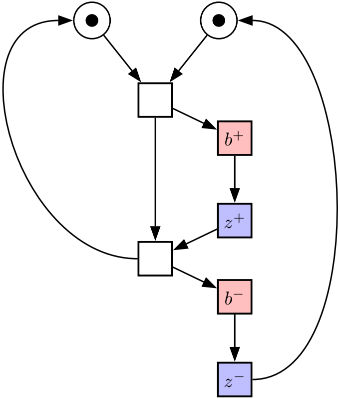

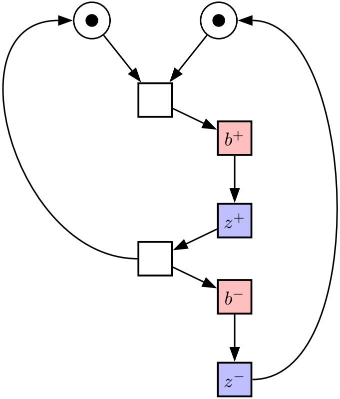

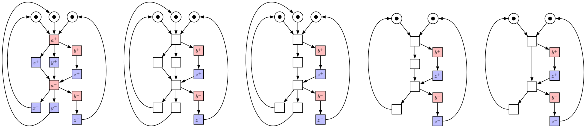

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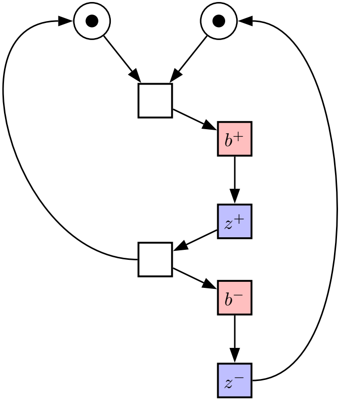

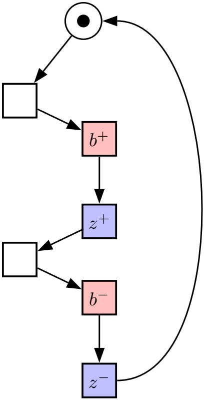

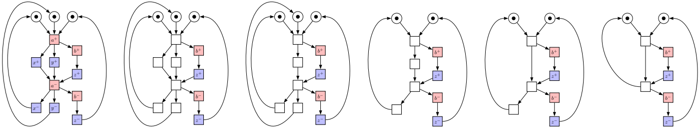

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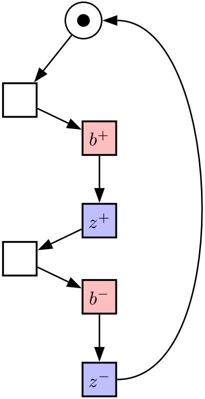

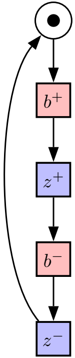

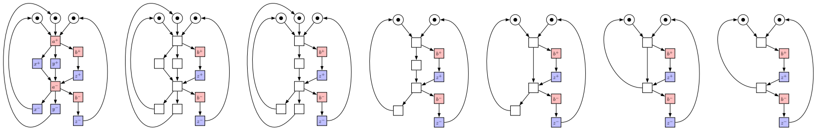

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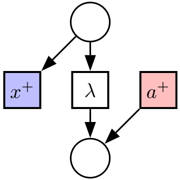
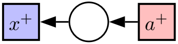
New Approach

- No backtracking for technical reasons
- λ transitions can be left in the component, as long as it is output-determinate (checked implicitly during synthesis)

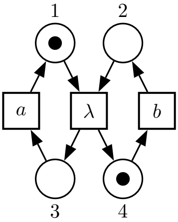
Decomposition – Non-Secure Contraction

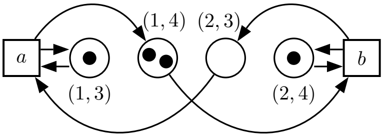




Language is changed

Decomposition – Non Safeness-Preserving Contraction





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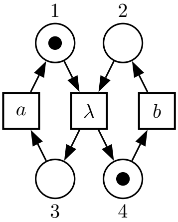
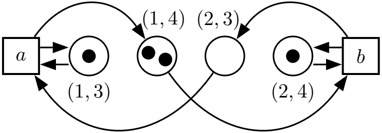
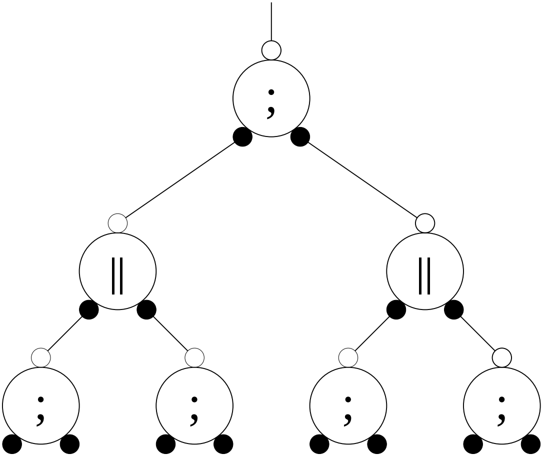




- Synthesis tools do not support non-safe STGs
- or just with a place capacity
- Latter is inefficient: every contraction doubles potential place capacity

Benchmarks — SeqParTree



Artificial Balsa Handshake component tree
of sequencers and parallelisers with 3 Levels

Benchmarks — Results

Level	$\lvert P\rvert - \lvert T\rvert$	$\lvert In\rvert - \lvert Out\rvert$	Old	New	Synthesis
5	382 – 252	33 – 93	1	1	5
6	798 – 508	65 – 189	4	4	16
7	1566 – 1020	129 – 381	9	8	22
8	3230 – 2044	257 – 765	32	17	1:02
9	6302 – 4092	513 – 1533	1:27	1:18	1:30
10	12958 – 8188	1025 – 3069	42:37	6:03	4:32

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Synthesis of an STG with 4094 signals in about 11 minutes.

More Results in the Paper

Deciding Output-Determinacy . . .

- PSPACE complete for bounded/safe STGs
- EXPSPACE hard for unbounded STGs

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Decomposition:

- Simplified correctness notion
- Decomposition can be applied to output-determinate (possibly) non-deterministic specifications
- More decomposition operations

Conclusion

Introduced output-determinacy

- Relaxation of determinism and determinacy
- Fits very well with STGs and speed-independency
- Allows a language-based semantics

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- Relaxation of determinism and determinacy
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Applied output-determinacy to STG decomposition

- Decomposition gets faster
- Allows more STG specifications
- More decomposition operations

Future Research and Related Work

Future Reseach

- Semantics for internal signals – application to output-determinacy and decomposition
- Decomposition works structurally only.
  Fast but problems with 'tricky' specifications
- Apply decomposition to BALSA resynthesis
- Preserving CSC in the components

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Related Work

- Carmona and Cortadella: ILP approach, e.g
  ILP models for the synthesis of asynchronous control circuits
- Myers and Yoneda: structural decomposition, e.g.
  Synthesis of Speed Independent Circuits Based on Decomposition